REMARKS

Applicants respectfully request favorable reconsideration of this application, as amended.

The abstract has been amended in accordance with the Examiner's recommendation.

Without acceding to the outstanding rejections, independent Claims 1, 2, 16, and 25 have been amended to recite features discussed hereinafter, with a number of the remaining claims having been editorially revised for clarity and consistency. The alleged informalities have been appropriately addressed. New Claims 35-47 have also been added, which correspond to Claims 3-15 but depend from Claim 1. Accordingly, Claims 1-47 are pending. At least as presently amended, the claims are believed to distinguish patentably from the prior art.

As amended, Claim 1 recites the following features: (i) in a first write operation for writing first data into a first area of the memory, the central processing unit writes the first data to a first portion of the first area, (ii) in a second write operation for writing second data into a second area of the memory, the central processing unit writes the second data to a portion of the second area, and (iii) the central processing unit writes supplemental information relating to the first data into a second portion of the first area in the first write operation, but does not write such supplemental information relating to the second data in the second write operation.

Independent Claim 2 recites that the central processing unit executes a predetermined process to thereby generate error correcting information and add the same to data to be written only for a specified partial storage area of the non-volatile memory and allow an error decision and an error correction based on the error correcting information to be effected on the data read from the specified partial storage area.

Independent Claim 16 recites a first storage area which is structured to allow for a relatively low number of rewrite assurances and a second storage area which is structured to allow for a relatively high number of rewrite assurances. Both the first storage area and second storage area are allocated in an address space of an arithmetic control device. The first storage area comprises programs which include an ECC code generating program for generating each of ECC codes for data to be written in the second storage area, and an error-correcting program for effecting an error decision and an error correction on data with the ECC codes read from the second storage area. The second storage area stores data and the ECC code for the data wherein the arithmetic control devices executes the ECC code generating program when data is stored in the second storage area.

Independent Claim 25, recites that a CPU stores data in memory cells at different addresses in a first memory area when information is written in the first memory area. The CPU also stores data in memory cells at different addresses

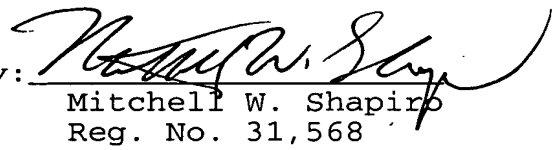
in a second memory area when information is written in the second memory area. Claim 25 further recites that for the first memory area, but not the second memory area, the CPU reads data from the memory cells at the different addresses, and performs a logical operation on the read plural data to thereby effect a necessary error correction to the data.

The outstanding Office Action cited numerous references to support various rejections under 35 U.S.C. § 103(a). However, none of the cited references teaches or suggests the above discussed subject matter of Applicants' invention as presently claimed.

An early Notice of Allowance is respectfully solicited.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

By: 

Mitchell W. Shapiro
Reg. No. 31,568

Jason H. Vick
Reg. No. 45,285

MWS:JHV:sjk

Miles & Stockbridge P.C.
1751 Pinnacle Drive, Suite 500
McLean, Virginia 22102-3833
(703) 903-9000

September 10, 2004